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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,035	04/20/2007	Tadahiro Ohmi	5016-0103PUS1	5997
2292	7590	02/07/2011	EXAMINER	
BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747				CALEY, MICHAEL H
ART UNIT		PAPER NUMBER		
2871				
NOTIFICATION DATE			DELIVERY MODE	
02/07/2011			ELECTRONIC	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/581,035	OHMI ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	MICHAEL H. CALEY	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 30 December 2010.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1,2,4-22 and 26-32 is/are pending in the application.  
 4a) Of the above claim(s) 12-22 and 26-31 is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1,2,4-11 and 32 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 30 May 2006 is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ .                                    |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____.   | 6) <input type="checkbox"/> Other: _____ .                        |

**DETAILED ACTION**

**Continued Examination Under 37 CFR 1.114**

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/30/10 has been entered.

**Claim Rejections - 35 USC § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

**Claims 1, 2, 5, 6, 9, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chino (U.S. Patent Application Publication No. 2004/0027056) in view of Odemura (JP 2001-188343A).**

Regarding claim 1, Chino discloses an active matrix display device having a plurality of thin film transistors disposed in a matrix on an insulating substrate and wiring connected to these thin film transistors;

wherein;

    said active matrix display device (Figures 1-2; Paragraphs [0051]-[0052]) comprises a flattening layer (element 9) surrounding said wiring (e.g. element 37), a surface of said wiring and a surface of said flattening layer forming substantially the same plane (Figures 2-4), and

    said active matrix display device further comprises an interlayer insulating film (59) on the plane formed by the surface of said wiring and the surface of said flattening layer, and a pixel electrode (20) on said interlayer insulating film.

Chino fails to disclose a material for the flattening layer. Odemura, however, teaches a flattening layer, such as those used in a liquid crystal display (Odemura: Paragraphs [0001], [0002], [0065], [0083]), as advantageously formed from a photosensitive resin composition (Odemura: abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the flattening layer from the proposed resin composition. One would have been motivated to form the flattening layer from the resin composition to benefit from its known

advantages for display use, such as high transparency, flatness, heat resistance, and chemical resistance (Odemura: abstract).

Regarding claim 2, Chino discloses said wiring as including gate wiring (35), source wiring (41), and drain wiring (37) being respectively connected to source and drain electrodes of the thin film transistor,

one of said source wiring and drain wiring constituting signal lines (37; Paragraph [0060]) adapted to supply signals to the thin film transistors while the other is connected to pixel electrodes (20; Paragraphs [0060]-[0061]),

and wherein the flattening layer surrounds the source electrodes, the drain electrodes, the source wiring, and the drain wiring (Figure 2),

surfaces of said source electrodes, said drain electrodes, said source wiring, and said drain wiring, and the surface of said flattening layer forming substantially the same plane (Figure 2).

Regarding claim 5, Chino as modified by Odemura discloses the flattening layer as comprising an inorganic substance (Odemura: e.g. Paragraphs [0027], [0033], [0042]).

Regarding claim 6, Chino as modified by Odemura discloses the flattening layer as formed by a alkali-soluble alicyclic olefin resin insulator composition having a radiation sensitive component (abstract).

Regarding claim 9, Chino discloses the insulating substrate as a substrate having a surface covered with an insulator (Figure 2 element 55).

Regarding claim 11, Chino discloses the display device as an organic EL display device (Paragraph [0098]).

**Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chino in view of Odemura and Ishihara et al. (U.S. Patent Application Publication No. 2002/0012080 "Ishihara").**

Chino fails to disclose an organic substance in the electrodes and wiring. Ishihara, however, teaches forming the electrodes and wiring to contain an organic substance (Paragraphs [0003], [0036], and [0061]-[0070]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the source and drain electrodes to contain an organic substance. One would have been motivated to form the source and drain electrodes with an organic substance to reduce the TFT panel production cost according to conventional means (Ishihara: Paragraph [0003]).

**Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chino in view of Odemura and in further view of Tanaka et al. (U.S. Patent No. 6,933,180 "Tanaka").**

Chino fails to disclose the display device as having a transparent substrate and as formed as a liquid crystal display. Tanaka, however, teaches TFT array substrates as interchangeably

implemented as for an organic EL display or a liquid crystal display (abstract; Column 1 lines 7-11) and the substrate as transparent (Column 4 lines 58-59).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the TFT array substrate as a liquid crystal display. One would have been motivated to form the display as a liquid crystal display to benefit from known advantages such as improved longevity and reduced production expense. Further, one would have been motivated to form the substrate to be transparent for allowing light from a light source, such as a backlight, to illuminate the display according to conventional means.

**Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chino in view of Odemura and Tanaka and in further view of Sakamoto et al. (U.S. Patent Application Publication No. 2003/0095217 “Sakamoto”).**

Chino fails to explicitly disclose the flattening layer as transparent. Sakamoto, however, teaches a transparent display insulating layer to allow light from a backlight to be transmitted through the liquid crystal layer and toward the viewer (Paragraph [0070]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the flattening layer as a transparent layer. One would have been motivated to form the flattening layer as a transparent layer to allow light to be passed.

### **Response to Arguments**

Applicant's arguments with respect to claims 1, 2, 4-11, and 32 have been considered but are moot in view of the new ground(s) of rejection.

### **Contact Information**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL H. CALEY whose telephone number is (571)272-2286. The examiner can normally be reached on M-F 6:00 a.m - 2:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael H. Caley/  
Primary Examiner, Art Unit 2871